Simple Two-Transistor Single-Supply Resistor-Capacitor Chaotic Oscillator

Lars Keuninckx, Guy Van der Sande and Jan Danckaert†

***Abstract*—We have modified an otherwise standard one-transistor self-biasing resistor-capacitor phase-shift oscillator to induce chaotic oscillations. The circuit uses only two transistors, no inductors, and is powered by a single supply voltage. As such it is an attractive and low-cost source of chaotic oscillations for many applications. We compare experimental results to Spice simulations, showing good agreement. We qualitatively explain the chaotic dynamics to stem from hysteretic jumps between unstable equilibria around which growing oscillations exist.**

***Index Terms*—chaos, oscillator. nonlinear dynamics, RC-ladder.**

I. Introduction

RECENTLY the interest in chaotic systems has been revived following the advent of novel and worthwhile applications. Chaotic systems are now being used for so-called chaos encryption, in which data signals can be secured by hiding them within a chaotic signal. Relying on chaos synchronization the original messages can then be safely recovered [1]. Also, the long-term unpredictability of the chaotic signal makes these systems well suited for true random bit generation [2]. In robotics, chaotic signals are being used in neural control networks or as chaotic path generators [3]. Finally, from a more fundamental point of view, a shift in interest towards networks of interconnected chaotic unit cells can be observed [4]. In all these applications, a need exists for flexible and preferably low cost chaotic circuits. Discrete components are preferable over operational amplifiers and specialized multiplier chips, the latter only being produced by a few suppliers. Single supply and low voltage operation widen the applicability, as does a wide easily tunable frequency range. Finally, using chaotic circuits as units in large networks adds the condition that the couplings between these units are dependable and stable. Requiring inductorless circuits will avoid such difficulties.

Since the development of Chua's circuit [5], there has been a considerable interest in the construction of autonomous chaotic circuits. Well known circuits, such as the Wien bridge oscillator, have been modified to produce chaos [6]. Often, these modifications involve the addition of an extra energy storage element such as an inductor at the right place, thereby adding a dimension to a predominantly two-dimensional limit cycle oscillator. In other cases, notably the Collpits oscillator [7], a chaotic regime is already present for certain values of the design parameters. Others directly translate a known chaotic system of differential equations to electronics. The necessary nonlinear terms are implemented by using dedicated analog multipliers as in reference [8] or operational amplifier based piece wise continious functions [9]. Being able to avoid operational amplifiers and dedicated multipliers is a plus in terms of cost and circuit complexity, as there is no connection between complexity -in terms of used parts- of the circuit and complexity of the chaotic oscillations -in terms of measurable quantitative properties such as entropy, attractor dimension, spectral content etc. Therefore chaotic oscillators using minimal and more basic components as in references [10] and [11] are desirable from an economic and logistic viewpoint.

Elwakil and Kennedy conjecture that every autonomous chaotic oscillator contains a core sinusoidal or relaxation oscillator [12]. Accordingly, one can derive a chaotic oscillator from any sinusoidal or relaxation oscillator. Motivated by this, we set out to modify the well known resistor-capacitor (RC) phase shift oscillator, described as early as 1941 in reference [13] to produce chaos. It has been used previously as the basis for chaotic circuits. Hosokawa *et al.* report on chaos in a system of two such oscillators, coupled by a diode [14]. They analyze the system as two nonlinearly coupled linear oscillators. Ogorzalek describes a chaotic RC phase shift oscillator based on a piecewise-linear amplifier built using operational amplifiers, however the RC-ladder is unmodified [15]. In our approach we use a transistor based RC oscillator to which a small subcircuit is added, directly interacting with the RC-ladder itself. The purpose of the subcircuit is to add a nonlinearity in the RC-ladder. The attractiveness of the resulting circuit lies in its simplicity and low cost and parts count. No specialized parts such as dedicated multipliers or rare inductor values are needed. Neither the component values nor the supply voltage is critical. The operation does not depend on the dynamic properties of the active components, as is often the case in even simpler chaotic circuits employing only one transistor. The main oscillating frequency has a range of over five decades, from below 1 Hz up to several hundred kilohertz. which can be reached by scaling the capacitors and/or resistors.

Additionally, the circuit has the attractive feature that the underlying core oscillator is clearly visible in the structure. This makes it a great introductory pedagogical tool for students interested in chaos.

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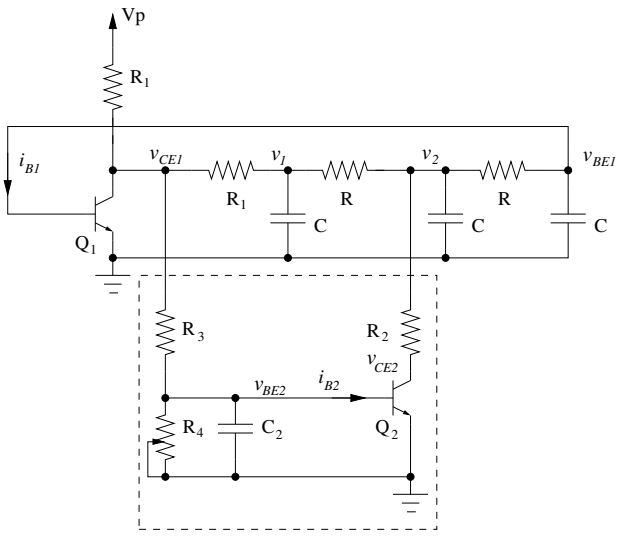


Figure 1. A two-transistor chaotic RC phase shift oscillator. The components in the dashed line box cause chaotic dynamics in an otherwise standard self biasing RC oscillator. The components have the following values: $R = 10\ \mathrm{k\Omega}$, $R_1 = 5\ \mathrm{k\Omega}$, $R_2 = 15\ \mathrm{k\Omega}$, $R_3 = 30\ \mathrm{k\Omega}$, $C = 1\ \mathrm{nF}$, $C_2 = 360\ \mathrm{pF}$, and $V_P = 5\ \mathrm{V}$.

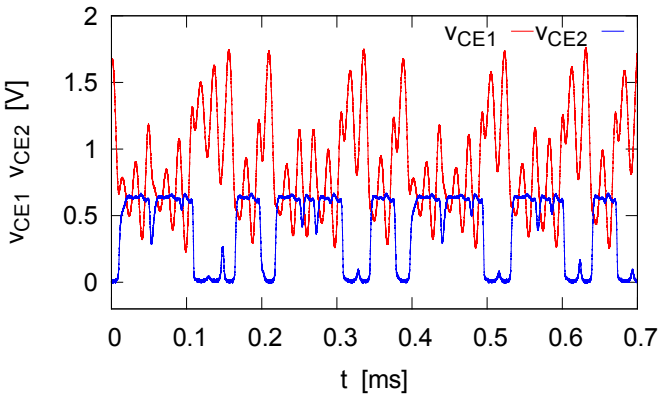


Figure 2. *Timetrace of v_{CE1} (upper trace, red in color) and v_{CE2} (lower trace, blue in color) for $R_4 = 44\ \mathrm{k\Omega}$, $V_p = 5\ \mathrm{V}$, other component values as stated in the text.*

II. Circuit and Experimental Results

Figure 1 introduces the circuit that we have designed. It consists of a standard single-supply self-biasing RC phaseshift oscillator with an added subcircuit (inside the dashed line box) interacting with the RC-ladder. Unless stated otherwise, the following component values are used: $R = 10\ \mathrm{k\Omega}$, $R_1 = 5\ \mathrm{k\Omega}$, $R_2 = 15\ \mathrm{k\Omega}$, $R_3 = 30\ \mathrm{k\Omega}$, $C = 1\ \mathrm{nF}$, $C_2 = 360\ \mathrm{pF}$. The transistors Q_1 and Q_2 are of the type BC547C although this is not critical. Both the first resistor of the RC-ladder and the collector resistor of transistor Q_1, have been chosen equal to $1/2R$. Since the output resistance of a common emitter amplifier roughly equals the collector resistor, the combined resistance equals R, thus forming the first resistor of the ladder. The frequency at which the RC-ladder has 180° phase lag necessary for oscillation, is given by $f = \sqrt{6}/2\pi RC \approx 39\ \mathrm{kHz}$. Due to the loading of the last RC stage by transistor Q_1's base, the free running frequency is shifted to $54\ \mathrm{kHz}$. The subcircuit consisting of Q_2, R_2, R_3, R_4 and C_2 is responsible for the chaotic behaviour. This subcircuit adds a new equilibrium in which transistor Q_1 is also biased as an active amplifier, enabling oscillations. It is clear that for low R_4 or low V_p, transistor Q_2 does not conduct and the circuit reduces to the unmodified phase shift oscillator. The base oscillation frequency in the chaotic operating regime for $R_4 = 44\ \mathrm{k\Omega}$, $V_p = 5\ \mathrm{V}$ is approximately $44\ \mathrm{kHz}$. The circuit consumes $3.1\ \mathrm{mW}$ at $5\ \mathrm{V}$. In Figure 2, we show the time trace of v_{CE1}. The dynamical behavior consists of jumps between two states of high and low voltage of the collector of Q_2. In between these jumps growing oscillations are observed on the collector of Q_1. Note that the collector voltage of Q_2 has an almost binary distribution. In Figure 3(a), we show an oscilloscope picture of v_{CE1} vs. v_{CE2} for $R_4 = 44\ \mathrm{k\Omega}$ and $V_p = 5\ \mathrm{V}$, from which the bistable oscillations around two unstable equilibria are clearly visible. Figures 3(b) and 3(c), showing v_{CE1} vs. v_2, and $v1$ vs. v_2 respectively, also attest to this, where the openings or 'eyes' of the attractor indicate a possible unstable equilibrium at their center. To estimate the largest Lyapunov exponent, we use the Time Series Analysis 'Tisean' package[16], from a timetrace consisting of 50000 points of v_{CE1}, representing $10\ \mathrm{ms}$, as $\lambda \approx (0.045 \pm 0.005)\ /\mu\mathrm{s}$. A positive Lyapunov exponent is a strong indication of chaotic dynamics. In Figure 4, we show oscilloscope pictures of v_1 vs. v_{CE1} for increasing values of R_4 at $V_p = 5\ \mathrm{V}$, indicates the evolution of the dynamics to chaos. For $R_4 = 0\ \mathrm{k\Omega}$ the subcircuit is inactive such that a simple limit cycle exists (not shown). Close to $R_4 = 30\ \mathrm{k\Omega}$ [Figure 4(a)] we see a period doubling bifurcation. At $R_4 = 31.6\ \mathrm{k\Omega}$ [Figure 4(b)] a critical slowing down occurs as shown by the point of high intensity on the analog oscilloscope picture. This value marks the onset of a bistable operation. Subsequent period doublings lead to chaos as seen in Figure 4(d) and Figure 4(e). The attractor consists of oscillations around two unstable equilibria with lower and higher average v_{CE1}. The asymmetry between the upper and lower opening of the attractors is caused by different average collector current of transistor Q_1, resulting in different gain. This asymmetry is seen regardless of which projection is chosen. Further increase of R_4 [Figure 4(f)] leads to a period halving sequence.

III. Model and Spice Simulation

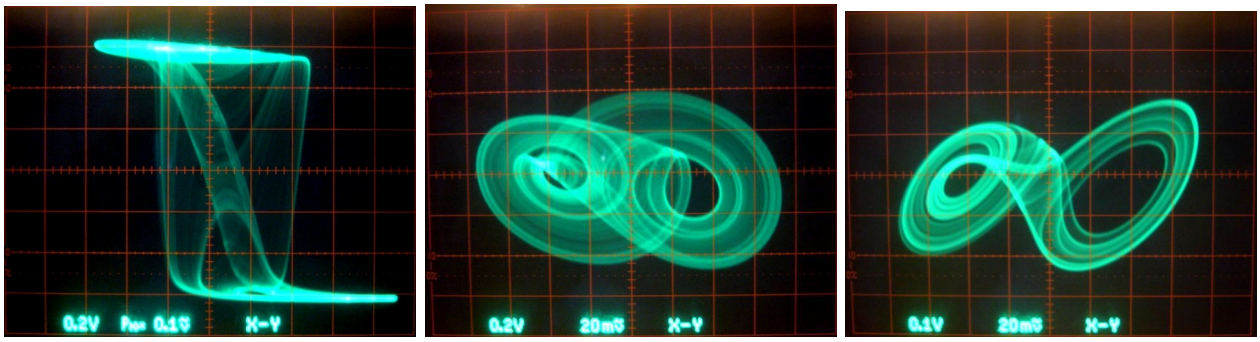
The circuit of Figure 1 is described by:

$$RC\frac{dv_1}{dt} = -v_1\left(1+\frac{R}{R_1}-\frac{RR_3}{R_1(2R_3+R_1)}\right) + v_2 + \frac{RR_3}{2R_3+R_1}\left(\frac{V_p}{R_1}-i_{C1}+\frac{v_{BE2}}{R_3}\right) \quad (1)$$

$$RC\frac{dv_2}{dt} = -2v_2 + v_1 + v_{BE1} - i_{C2}R, \quad (2)$$

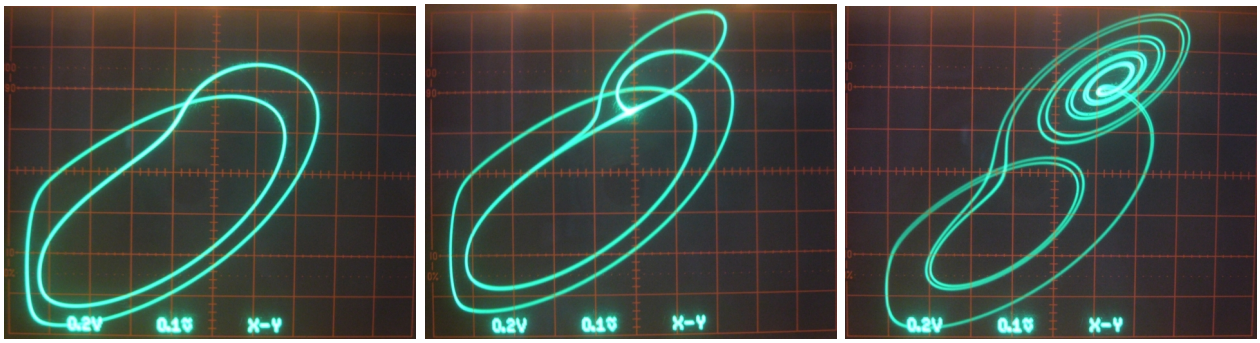
$$RC\frac{dv_{BE1}}{dt} = -v_{BE1} + v_2 - i_{B1}R, \quad (3)$$

$$(2R_3+R_1)\,C_2\frac{dv_{BE2}}{dt} = -v_{BE2}\left(2+\frac{2R_3+R_1}{R_4}\right) + v_1 + V_p - i_{C1}R_1 - i_{B2}\,(2R_3+R_1)\,. \quad (4)$$

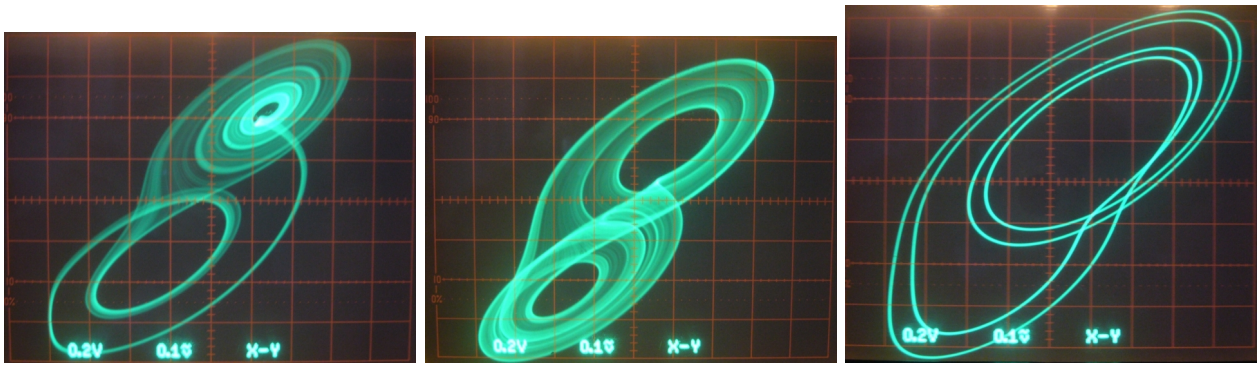


(a) (b) (c)

Figure 3. Attractor projections from the circuit for $R_4 = 44$ kΩ, $V_p = 5$ V. (a) horizontal: v_{CE1}, 0.2 V/div, vertical: v_{CE2}, 0.1 V/div, (b) horizontal: v_{CE1}, 0.2 V/div, vertical: v_2, 20 mV/div, (c) horizontal: v_1, 0.1 V/div, vertical: v_2, 20 mV/div.



(a) $R_4 = 30$ kΩ. (b) $R_4 = 31.6$ kΩ. (c) $R_4 = 37.5$ kΩ.



(d) $R_4 = 39.5$ kΩ. (e) $R_4 = 44$ kΩ. (f) $R_4 = 75$ kΩ.

Figure 4. The route to chaos. Horizontal: v_{CE1}, vertical: v_1 for increasing values of R_4 at $V_p = 5$ V. The asymmetry between the upper and lower 'eye' of the attractors is caused by different average collector current of Q_1, resulting in different gain.

The currents i_{B1}, i_{B2}, i_{C1} and i_{C2} are determined by the transistor model and are a function of the base-emitter and collector voltages v_{BE1}, v_{BE2}, v_{CE1} and v_{CE2}. These form the nonlinearities in the circuit. Note R_2 is absent from (1)-(4), however since $v_{CE2} = v_2 - i_{CE2}R_2$, current i_{C2} is influenced by R_2. In Figure 5, we show timetraces of v_{CE1} and v_{CE2} as generated from Spice. These again show bistable oscillations for v_{CE1} and jumping between a high and a low state for v_{CE2} and have a good qualitative agreement with the measurements in Figure 2. In Figure 6, a three dimensional plot of this simulation adding v_1 as third variable, is shown with color intensity coding used to indicate time from orange (beginning of the simulation) to light yellow (towards the end of the simulation). The bistable nature of the circuit in this operating regime is clear. A projection on the v_{CE1}-v_1 plane is shown for comparison with Figure 4(e). Figure 7(a) shows the one dimensional bifurcation diagram of v_{CE1} for parameter R_4, with $V_p = 5$ V, where the dynamics start for low values of R_4 with a limit cycle, evolving to chaos at $R_4 \approx 45$ kΩ through period doubling bifurcations. The chaotic dynamics are interspersed with small periodic windows indicating the possible co-existance of a chaotic attractor with a limit cycle. Similar results can be obtained by varying R_3 while keeping other parameters fixed. In general it must be noted that the location of the features in these plots depends much on the transistor model, even for the same type of transistor, as

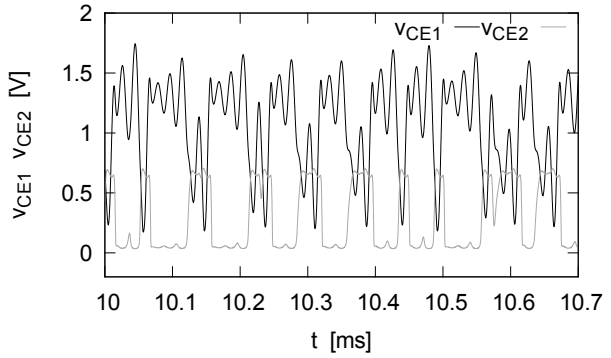


Figure 5. v_{CE1} (black) and v_{CE2} (grey) via Spice simulation for $R_4 = 44$ kΩ and $V_p = 5$ V.

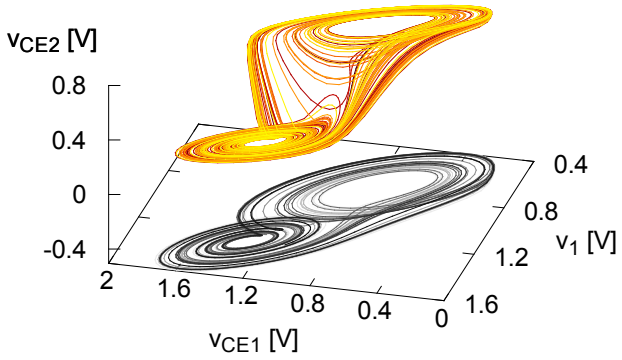


Figure 6. A three dimensional view of the attractor at $V_p = 5$ V and $R_4 = 44$ kΩ, generated from a 5 ms Spice generated timeseries in 100 ns increments. Coloring intensity indicates transistion time during the simulation, from orange at the beginning, to light yellow, near the end of the simulation.

these models differ somewhat per manufacturer. Figure 7(b) indicates that the circuit can produce chaos over a wide range of supply voltages as confirmed in our experiments.

IV. The 'Hidden' Bistable Circuit

Here we offer a qualitative explanation for the appearance of chaos in this circuit. Intuitively the circuit can be understood as a Schmitt-trigger combined with an oscillator as follows. If one removes capacitors C from Figure 1 as in Figure 8, one ends up with a circuit in which there is only one energy storing element, C_2. The node voltages in equilibrium of this one dimensional circuit equal those of the original four dimensional circuit. Often when a circuit shows bistability, in at least one of the states the active components are either saturated or non-conducting such that there is no gain available to support oscillation. We now show that transistor Q_1 has gain in both states. Consider the circuit with capacitors C removed as described above. Intuitively, if $v_{BE2} < 0.6$ V, Q_2 is non conducting, then $v_{CE1} \approx v_{BE1} \approx 0.6$ V. If by some external disturbance or a variation of R_4, v_{BE2} rises above ≈ 0.6 V, Q_2 will begin to conduct. Consequently v_{BE1} decreases, resulting in an increase of v_{CE1}, increasing v_{BE2}, etc. until Q_2 is saturated. At this point, with the choice of components where $R_1 + R = R_2$, we have $v_{CE1} \approx 2 \times 0.6$ V.

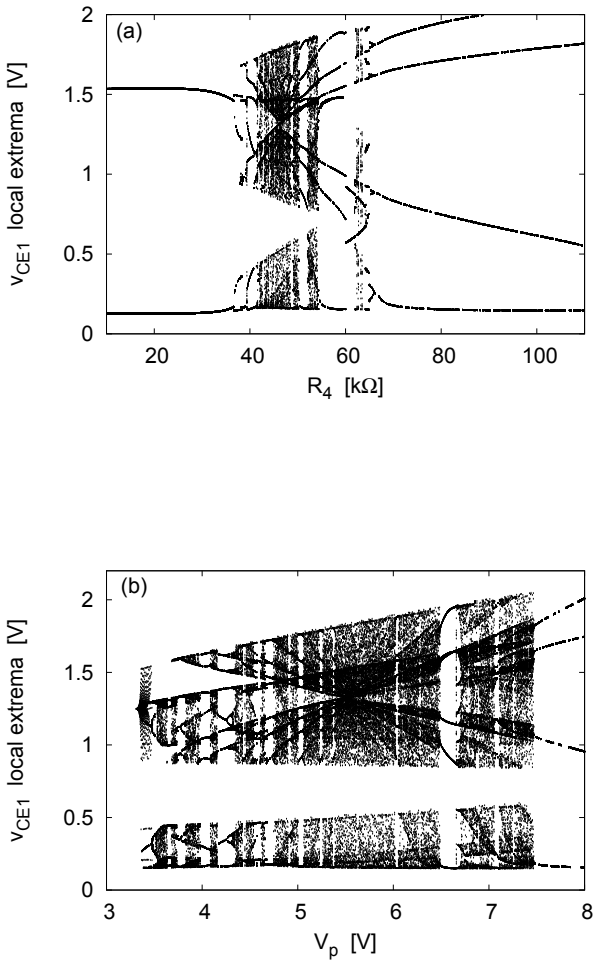


Figure 7. One dimensional bifurcation diagrams generated from Spice data. (a) over R_4 with $Vp = 5$ V , (b) over V_p for $R_4 = 44$ kΩ. Both plots show period doubling routes to chaos, periodic windows and crises.

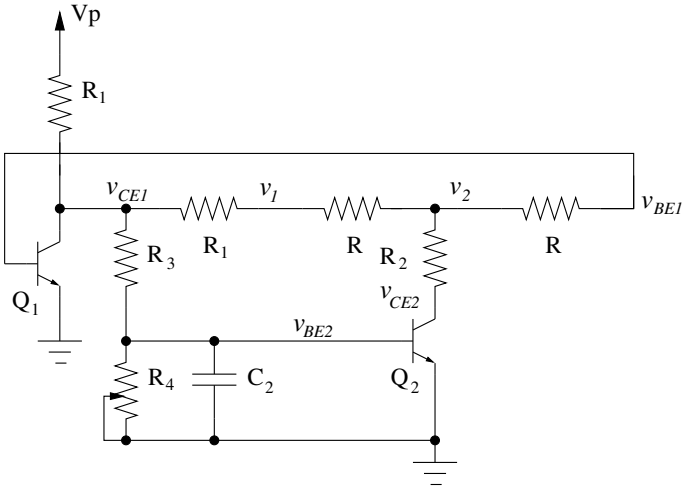


Figure 8. By removing the capacitors C associated with the oscillator in Figure 1, the embedded bistable circuit becomes visible.

Thus intuitively there two states exist, distinguished by Q_2 being either conducting or not, while Q_1 is biased as an active amplifier in both states. These states are stable for the circuit of Figure 8. In the case of the full four dimensional circuit however, these states are unstable and form the centers of the observed oscillations. Indeed both experimentally and numerically we find that transistor Q_2 is most of the time either non conducting or saturated, as shown in Figure 2. Hysteretic jumping as a basis of chaotic dynamics has been found in other chaotic oscillators, as described in references [17] and [18].

V. Discussion

A chaotic oscillator derived from a self biasing discrete resistor-capacitor ladder oscillator has been introduced. The circuit does not need specialty components and operates from a single supply voltage. It has a wide frequency range which can be chosen by scaling the capacitors and/or resistors. Therefore it is suited for many applications such as robotics, random number generators and chaos encryption. Being inductorless and thus avoiding hard-to-manage magnetic couplings between nearby units, it also lends itself well for research into the dynamics of chaotic networks. Spice simulations confirm the chaotic dynamics found experimentally. Intuitively the circuit can be explained as an oscillator modified such that growing oscillations exist around two unstable fixed points, with hysteretic jumping between them.

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